V_{DRM} = 5200 V
$I_{T(AV)M}$ = 3720 A
$I_{T(RMS)}$ = 5840 A
I_{TSM} = $63.0 \cdot 10^3$ A
V_{T0} = 0.96 V
r_T = 0.194 mΩ

Phase Control Thyristor

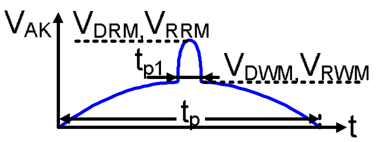
5STP 34Q5200

Doc. No. 5SYA1052-07 Apr. 20

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

Blocking

***Maximum rated values* 1)**

Parameter	Symbol	Conditions	5STP 34Q5200	Unit
Max. surge peak forward and reverse blocking voltage	V_{DSM}, V_{RSM}	t_p = 10 ms, f = 5 Hz T_{vj} = 5…125 °C, Note 1	5200	V
Max repetitive peak forward and reverse blocking voltage	V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms, t_{p1} = 250 µs, T_{vj} = 5…125 °C, Note 1, Note 2	5200	V
Max crest working forward and reverse voltages	V_{DWM}, V_{RWM}		3470	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to 0.67·V_{DRM}, T_{vj} = 125 °C	2000	V/µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	V_{DRM}, T_{vj} = 125 °C			500	mA
Reverse leakage current	I_{RRM}	V_{RRM}, T_{vj} = 125 °C			500	mA

Note 1: Voltage de-rating factor of 0.11% per °C is applicable for T_{vj} below +5 °C.
Note 2: Recommended minimum ratio of V_{DRM} / V_{DWM} or V_{RRM} / V_{RWM} = 2. See App. Note 5SYA 2051.

Mechanical data

***Maximum rated values* 1)**

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		81	90	108	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				2.1	kg
Housing thickness	H	F_M = 90 kN, T_a = 25 °C	26.25		26.70	mm
Surface creepage distance	D_S		36			mm
Air strike distance	D_a		15			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

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On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, Tc = 70 °C			3720	A
RMS on-state current	$I_{T(RMS)}$				5840	A
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, $V_D = V_R$= 0 V, after surge			$63.0 \cdot 10^3$	A
Limiting load integral	I^2t				$19.8 \cdot 10^6$	A^2s
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, $V_R = 0.6 \cdot V_{RRM}$, after surge			$45.5 \cdot 10^3$	A
Limiting load integral	I^2t				$10.3 \cdot 10^6$	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 3000 A, T_{vj} = 125 °C		1.47	1.54	V
Threshold voltage	$V_{(T0)}$	I_T = 2300 A - 7000 A, T_{vj} = 125 °C			0.96	V
Slope resistance	r_T				0.194	mΩ
Holding current	I_H	T_{vj} = 25 °C			125	mA
		T_{vj} = 125 °C			75	mA
Latching current	I_L	T_{vj} = 25 °C			500	mA
		T_{vj} = 125 °C			250	mA

Switching

Maximum rated values [1)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_{vj} = 125 °C, I_T = 3000 A, $V_D \leq 0.67 \cdot V_{DRM}$, I_{GM} = 2 A, t_r = 0.5 µs	Cont. f = 50 Hz			250	A/µs
			Cont. f = 1 Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 125 °C, I_T = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20 V/µs				700	µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	T_{vj} = 125 °C, I_T = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs	3400	4770	5200	µAs
Reverse recovery current	I_{RM}		60	77	95	A
Gate turn-on delay time	t_{gd}	T_{vj} = 25 °C, $V_D = 0.4 \cdot V_{RM}$, I_{GM} = 2 A, t_r = 0.5 µs			3	µs

Triggering

***Maximum rated values* [1)]**

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 7			W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	T_{vj} = 25 °C			2.6	V
Gate-trigger current	I_{GT}	T_{vj} = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			0.3	V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			10	mA

Thermal

***Maximum rated values* [1)]**

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case	$R_{th(j-c)}$	Double-side cooled F_m = 81... 108 kN			5	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 81... 108 kN			10	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 81... 108 kN			10	K/kW
Thermal resistance case to heatsink	$R_{th(c-h)}$	Double-side cooled F_m = 81... 108 kN			1	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 81... 108 kN			2	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	3.563	0.905	0.514	0.018
τ_i(s)	0.4587	0.0526	0.0055	0.0007

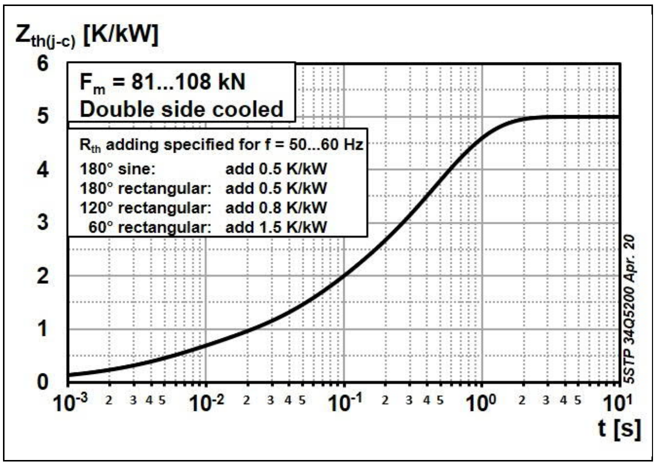

Fig. 1 Transient thermal impedance (junction-to-case) vs. time

Max. on-state characteristic model:

$$V_{T25} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 1000 - 70000 A

A_{25}	B_{25}	C_{25}	D_{25}
$2.02 \cdot 10^{-1}$	$1.14 \cdot 10^{-4}$	$1.20 \cdot 10^{-1}$	$2.16 \cdot 10^{-3}$

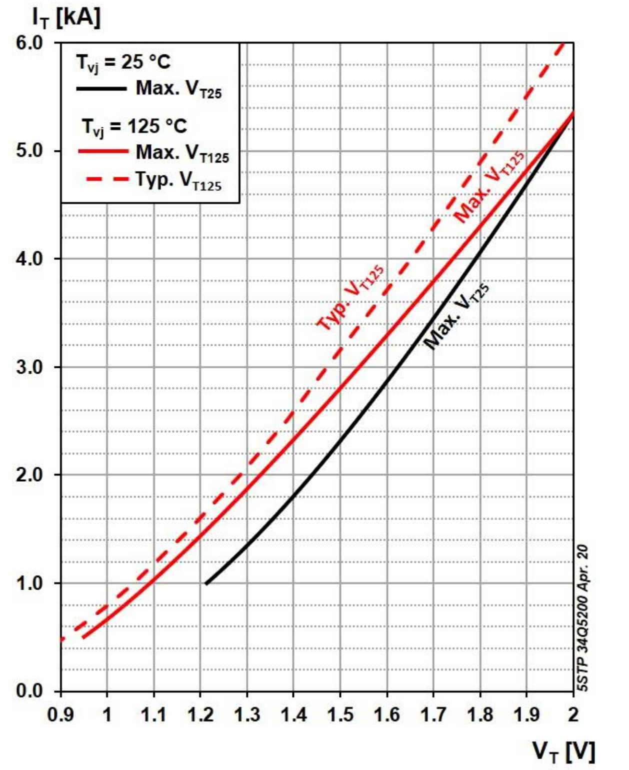

Fig. 2 On-state voltage characteristics

Max. on-state characteristic model:

$$V_{T125} = A_{Tvj} + B_{Tvj} \cdot I_T + C_{Tvj} \cdot \ln(I_T + 1) + D_{Tvj} \cdot \sqrt{I_T}$$

Valid for I_T = 500 - 70000 A

A_{125}	B_{125}	C_{125}	D_{125}
$5.69 \cdot 10^{-1}$	$1.49 \cdot 10^{-4}$	$3.14 \cdot 10^{-2}$	$5.00 \cdot 10^{-3}$

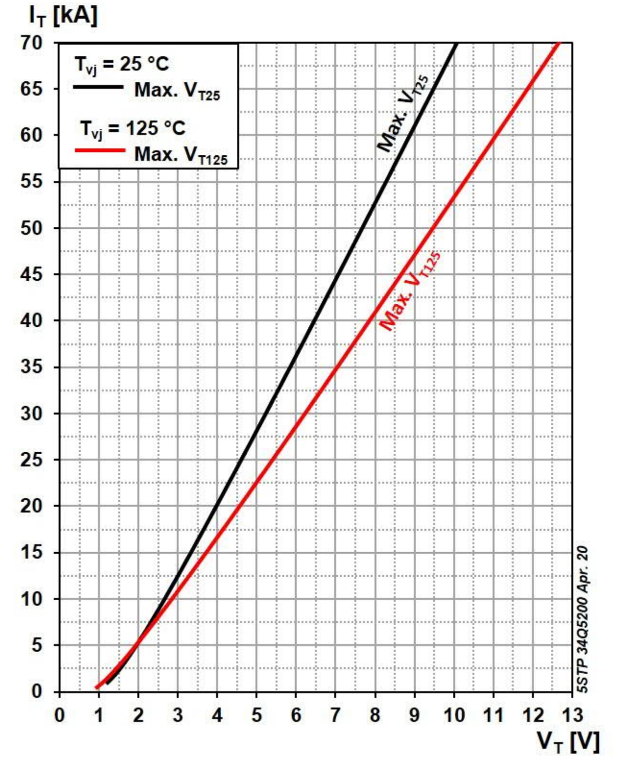

Fig. 3 On-state voltage characteristics

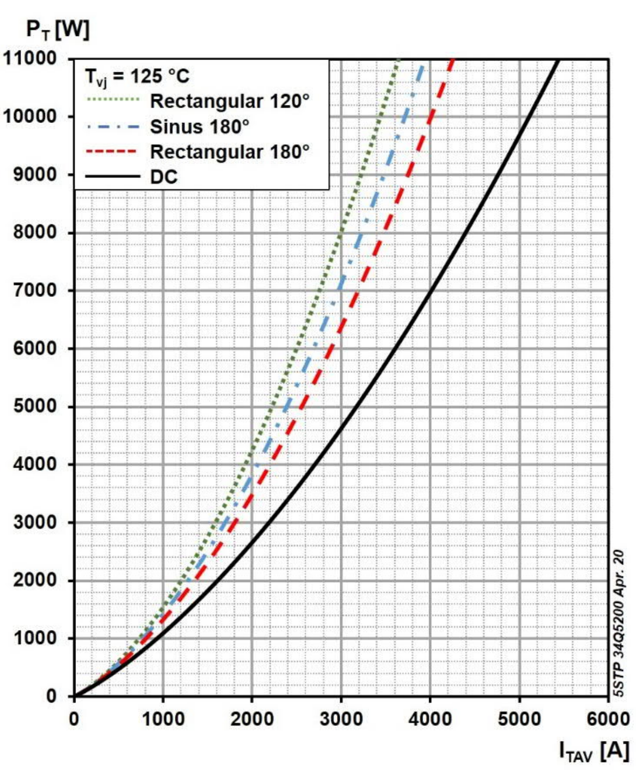

Fig. 4 On-state power dissipation vs. mean on-state current, turn-on losses excluded

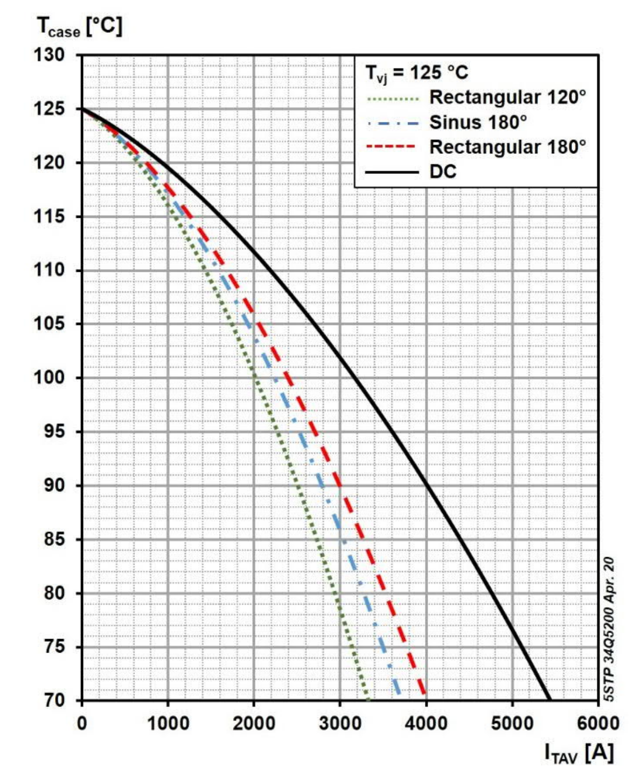

Fig. 5 Max. permissible case temperature vs. mean on-state current, switching losses ignored

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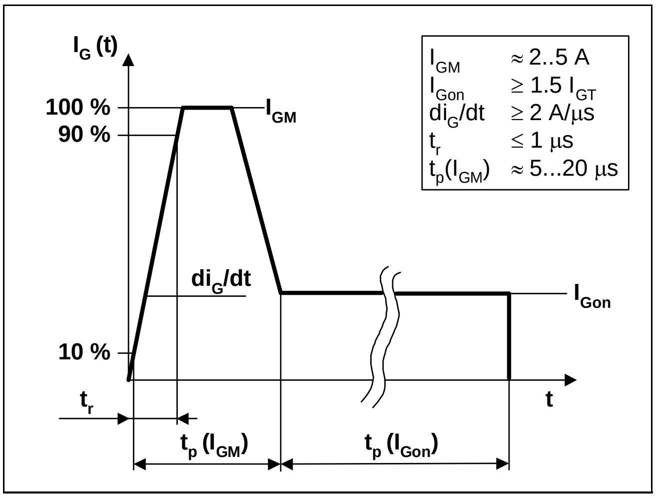

Fig. 6 Recommended gate current waveform

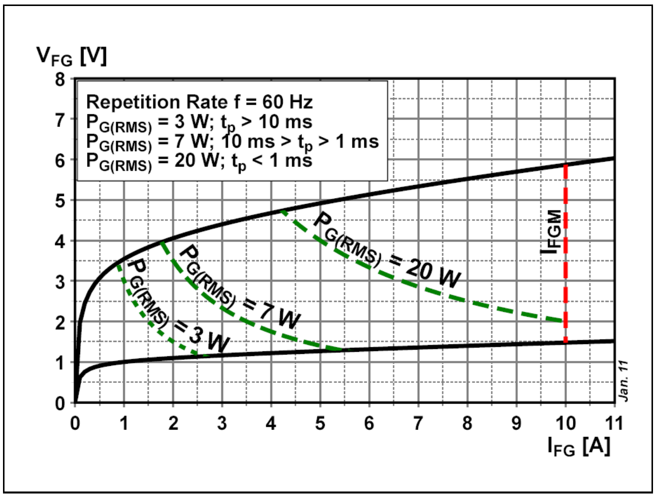

Fig. 7 Max. peak gate power loss

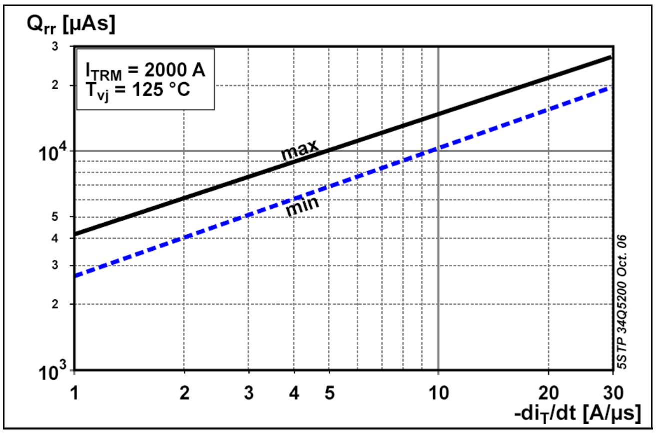

Fig. 8 Reverse recovery charge vs. decay rate of on-state current

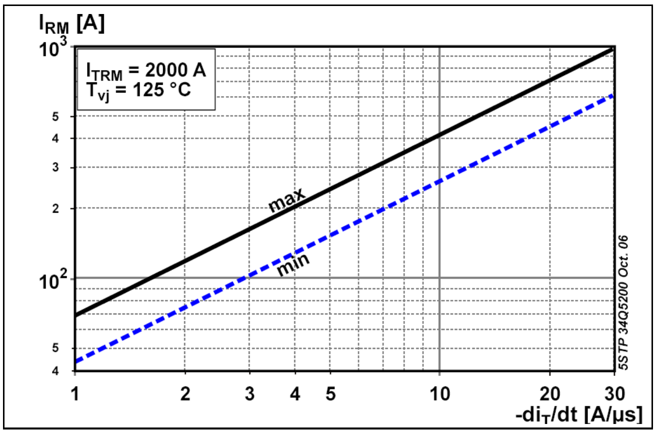

Fig. 9 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

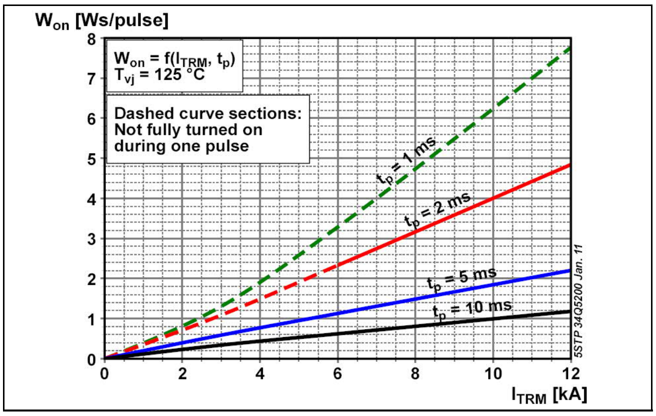

Fig. 10 Turn-on energy, half sinusoidal waves

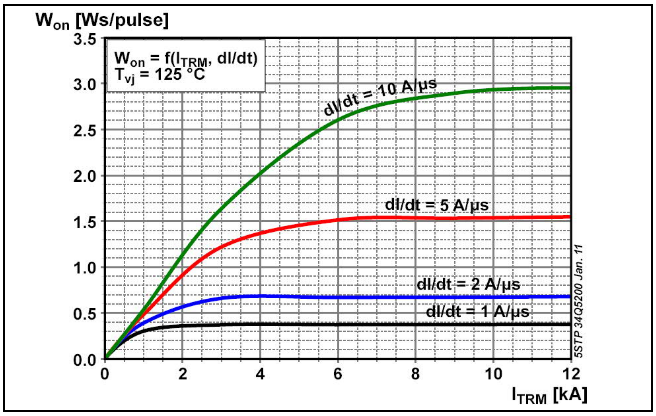

Fig. 11 Turn-on energy, rectangular waves

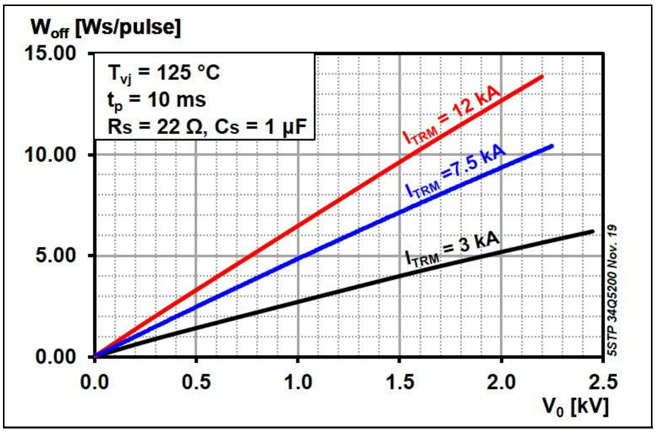

Fig. 12 Typical turn-off energy, half sinusoidal waves

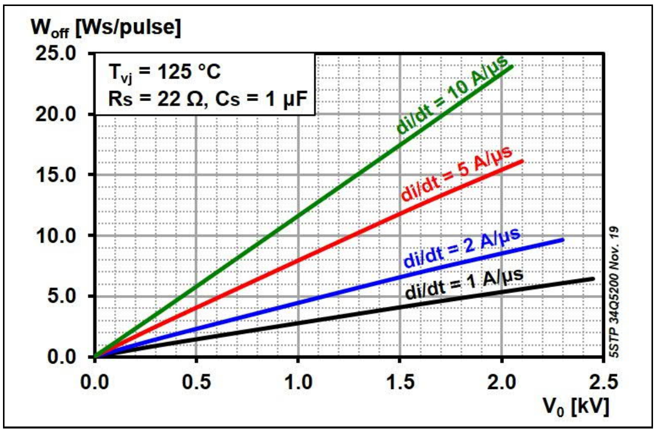

Fig. 13 Typical turn-off energy, rectangular waves

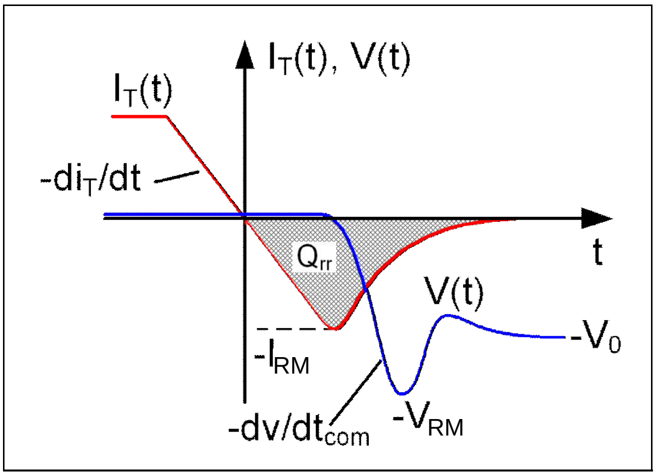

Fig. 14 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T}\int_0^T I_T \cdot V_T(I_T)\ dt$$

Fig. 15 Relationships for power loss

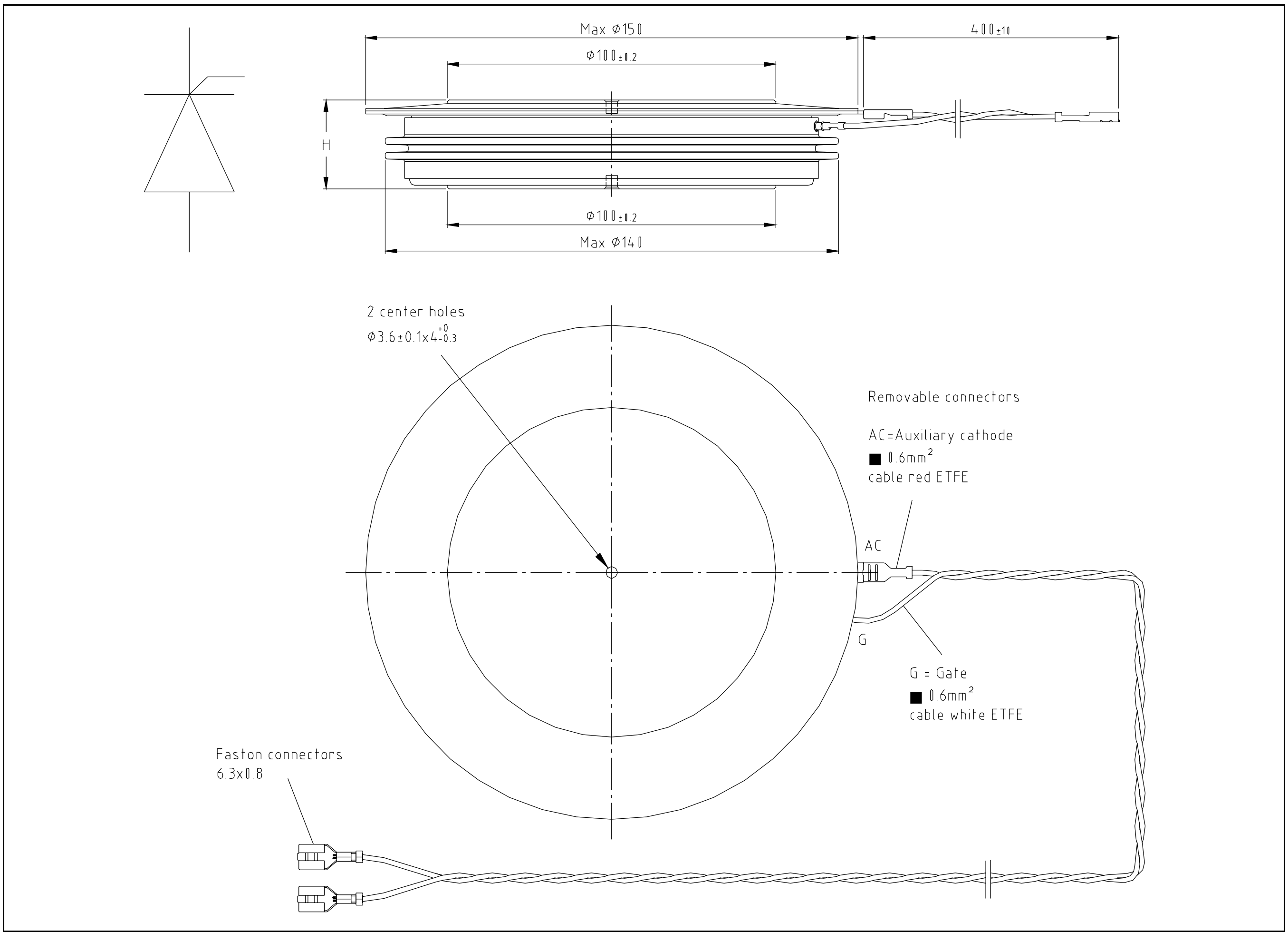

Fig. 16 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubbers for Phase Control Applications
5SYA 2049	Voltage definitions for phase control and bi-directionally controlled thyristors
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-drive recommendations for phase control and bi-directionally controlled thyristors
5SYA 2036	Recommendations regarding mechanical clamping of Press-Pack High Power Semiconductors
5SYA 2102	Surge currents for Phase Control Thyristors
5SZK 9118	General Environmental Conditions for High Power Semiconductors

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